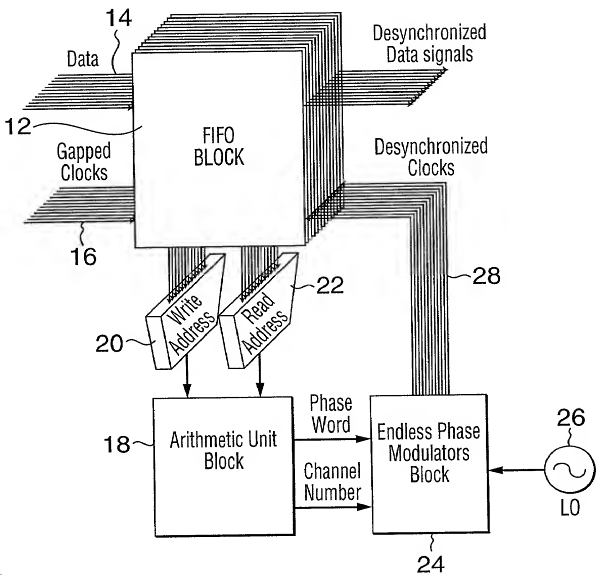
14
Data
12
Gapped
Clocks
16
FIFO
BLOCK
Desynchronized
Data signals
Desynchronized
Clocks
28
22
Write
Address
Read
Address
20
18
Arithmetic Unit
Block
Phase
Word
Channel
Number
Endless Phase
Modulators
Block
24
26
LO

FIG. 1

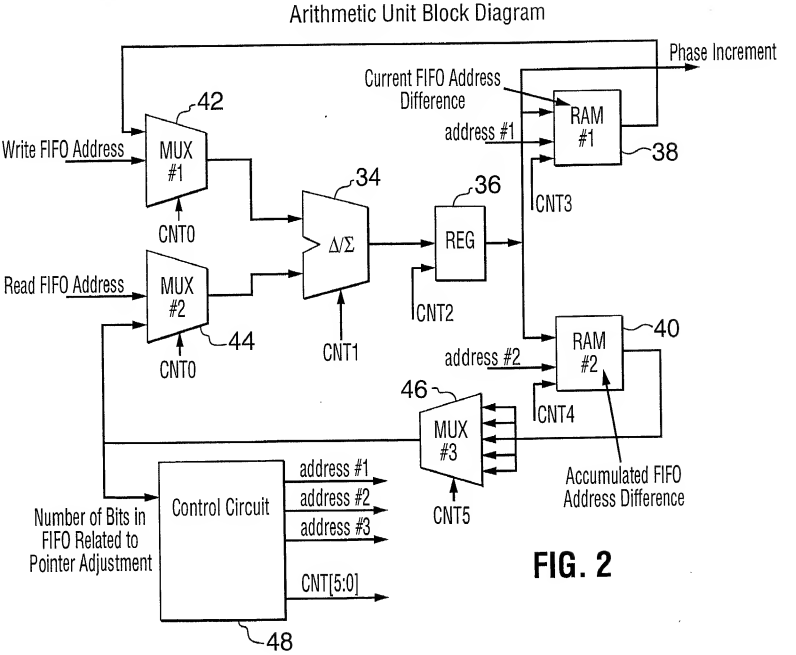

FIG. 2

Memory Map of RAM#1 for desynchronizing 12 channels of DS3 signal dropped from OC-12 signal

Ch#1 FIFO Address Difference
Ch#2 FIFO Address Difference
Ch#3 FIFO Address Difference
Ch#4 FIFO Address Difference
Ch#5 FIFO Address Difference
Ch#6 FIFO Address Difference
Ch#7 FIFO Address Difference
Ch#8 FIFO Address Difference
Ch#9 FIFO Address Difference
Ch#10 FIFO Address Difference
Ch#11 FIFO Address Difference
Ch#12 FIFO Address Difference
0
8
1/64 of UI Phase Increment
1/64

NOTE: N can be chosen for specific leak rate. Few more addresses can be added to the Ram#1 address space to enable adaptive bit leak rate!

Memory Map of RAM#2 for desynchronizing 12 channels of DS3 signal dropped from OC-12 signal

Ch#1 Accumulated FIFO Address Difference
Ch#2 Accumulated FIFO Address Difference
Ch#3 Accumulated FIFO Address Difference
Ch#4 Accumulated FIFO Address Difference
Ch#5 Accumulated FIFO Address Difference
Ch#6 Accumulated FIFO Address Difference
Ch#7 Accumulated FIFO Address Difference
Ch#8 Accumulated FIFO Address Difference
Ch#9 Accumulated FIFO Address Difference
Ch#10 Accumulated FIFO Address Difference
Ch#11 Accumulated FIFO Address Difference
Ch#12 Accumulated FIFO Address Difference
Ch#1 Pointer Adjustment Bits #
Ch#2 Pointer Adjustment Bits #
Ch#3 Pointer Adjustment Bits #
Ch#4 Pointer Adjustment Bits #
Ch#5 Pointer Adjustment Bits #
Ch#6 Pointer Adjustment Bits #
Ch#7 Pointer Adjustment Bits #
Ch#8 Pointer Adjustment Bits #
Ch#9 Pointer Adjustment Bits #
Ch#10 Pointer Adjustment Bits #
Ch#11 Pointer Adjustment Bits #
Ch#12 Pointer Adjustment Bits #
Spare Address for Holding Intermediate Values

FIG. 3

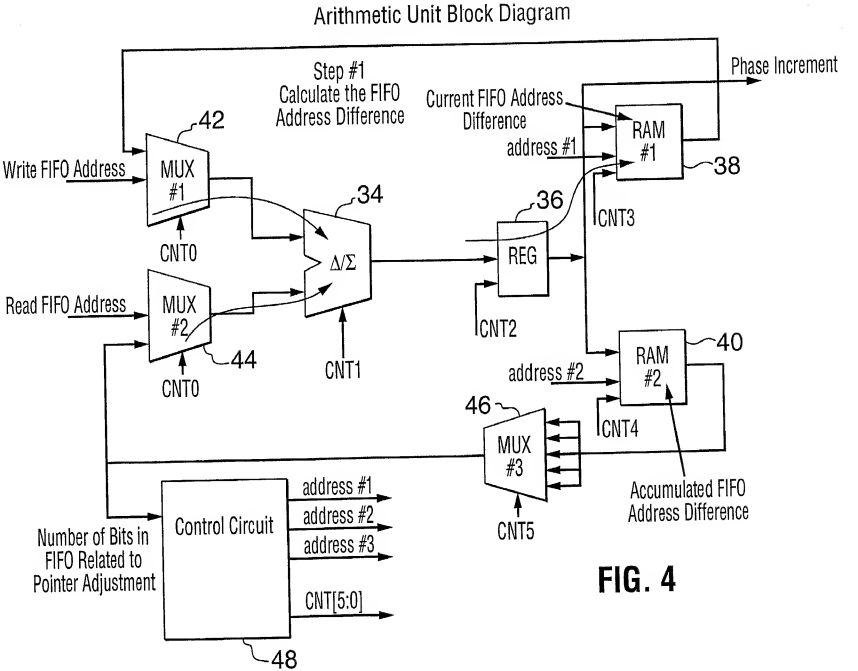

FIG. 4

Arithmetic Unit Block Diagram

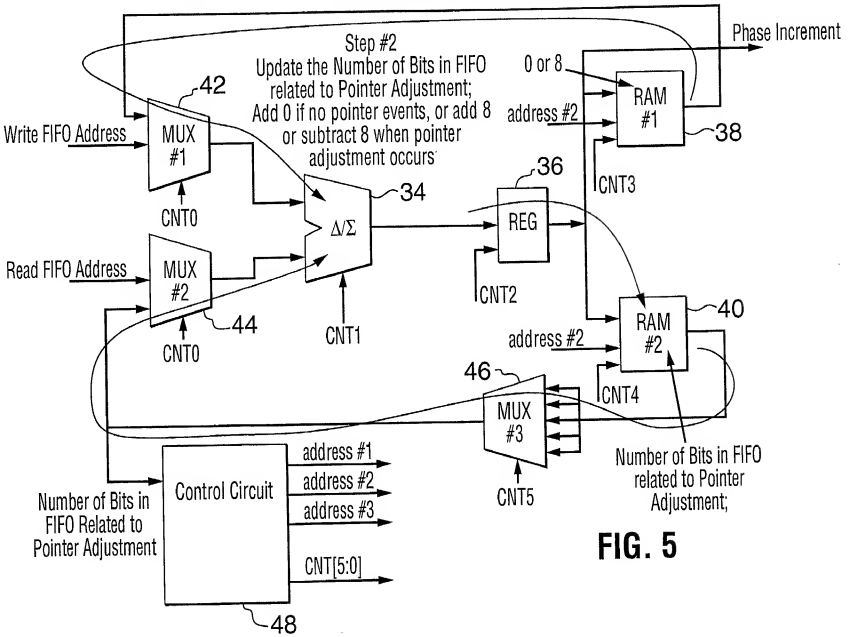

FIG. 5

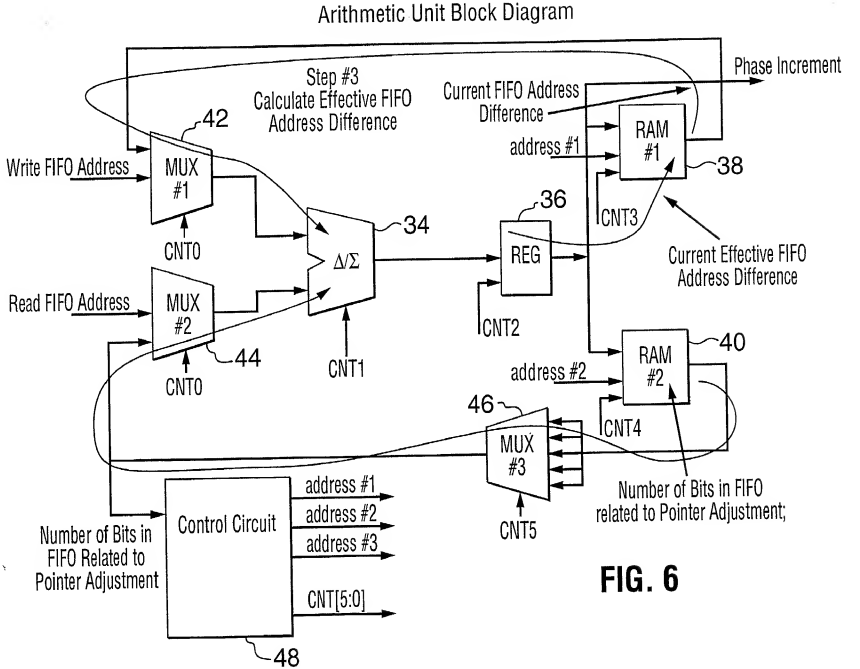

FIG. 6

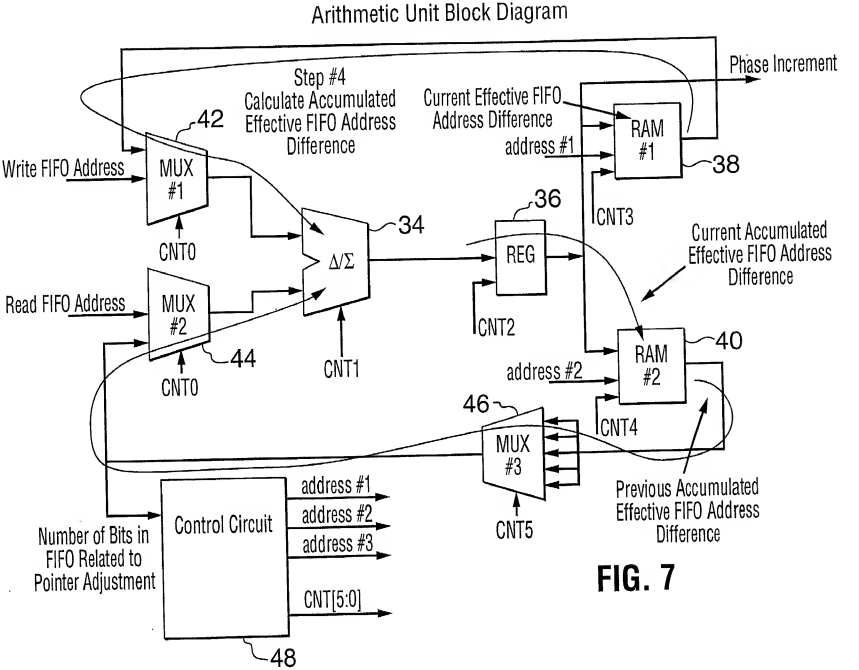

FIG. 7

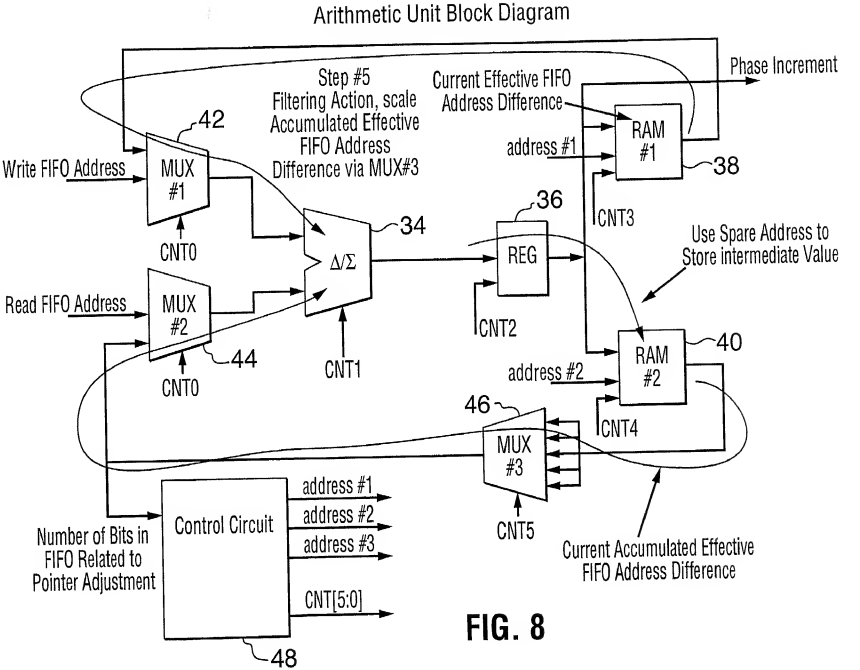

FIG. 8

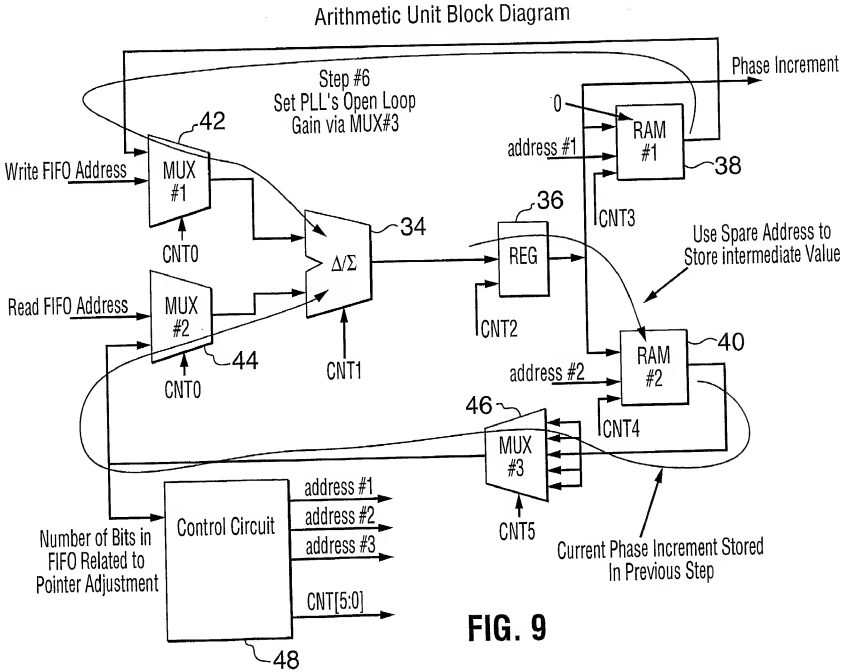

FIG. 9

Arithmetic Unit Block Diagram

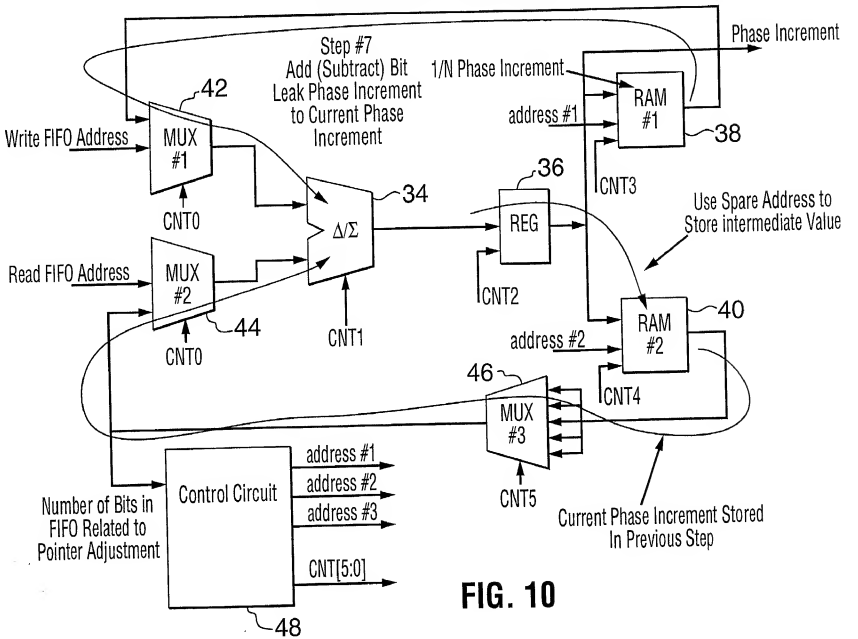

FIG. 10

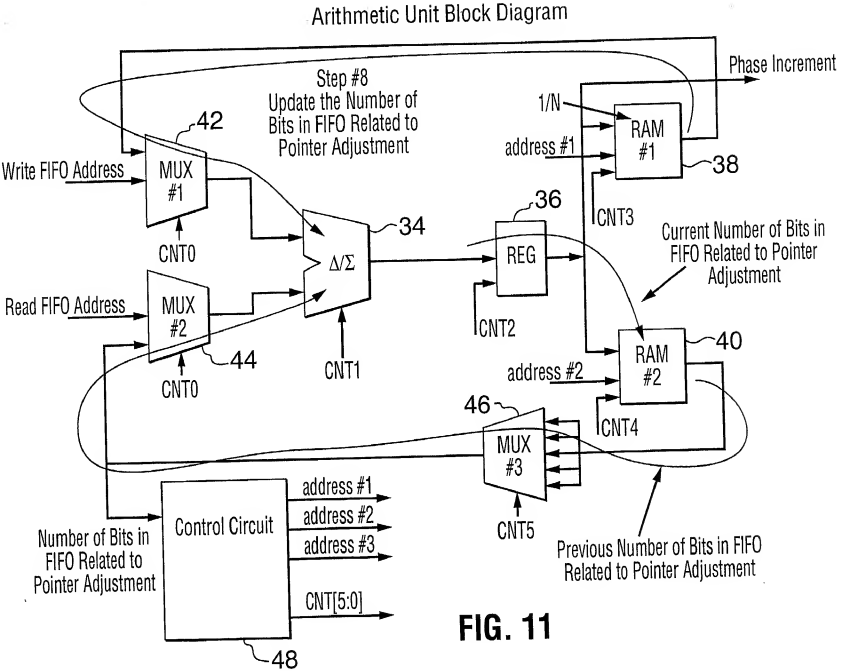

FIG. 11

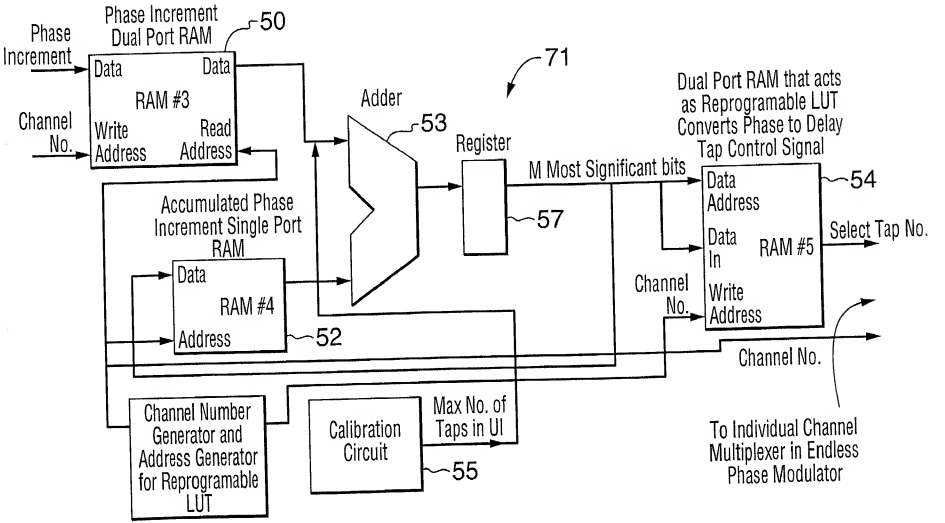

FIG. 12

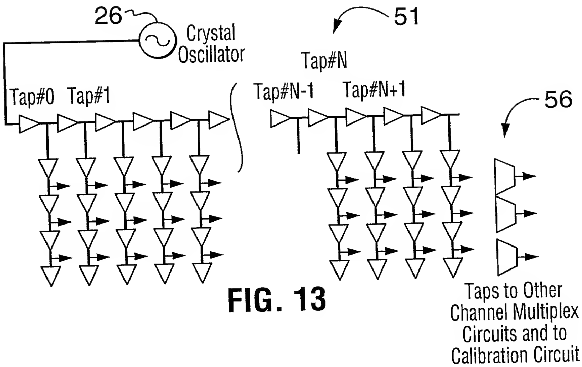
26
Crystal Oscillator
51
Tap#N
Tap#0
Tap#1
Tap#N-1
Tap#N+1
56
Taps to Other Channel Multiplex Circuits and to Calibration Circuit

FIG. 13

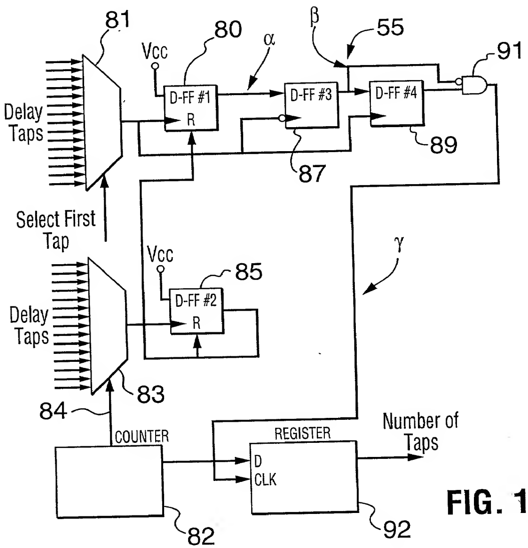
81
80
Vcc
α
β
55
91
D-FF #1
R
D-FF #3
D-FF #4
Delay Taps
89
87
Select First Tap
γ
Vcc
85
D-FF #2
R
Delay Taps
83
84
COUNTER
REGISTER
Number of Taps
D
CLK
82
92

FIG. 14

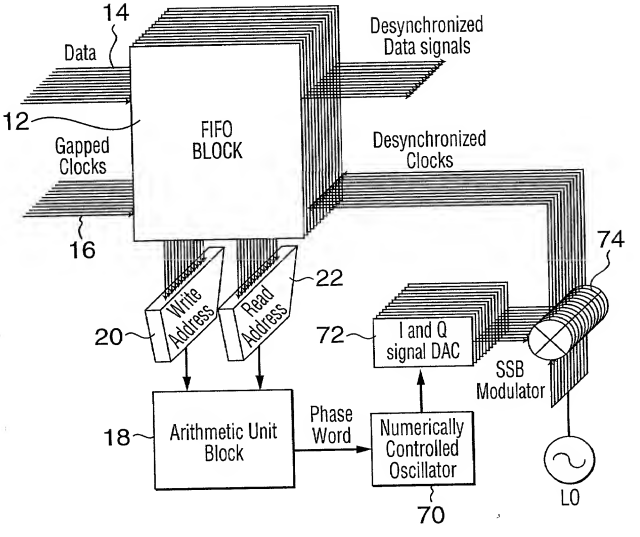

FIG. 15

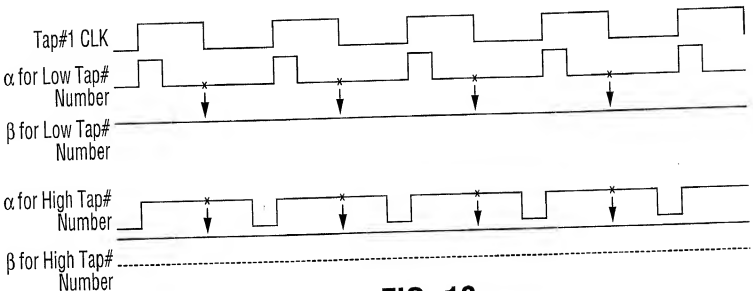

FIG. 16

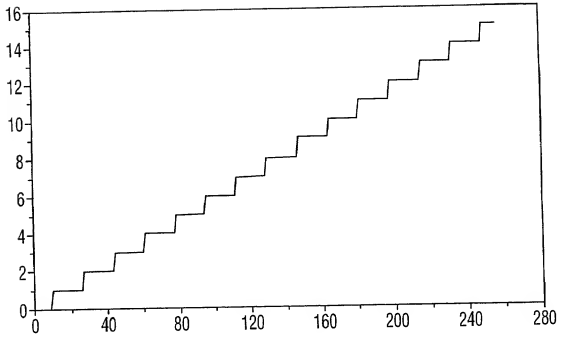

FIG. 17

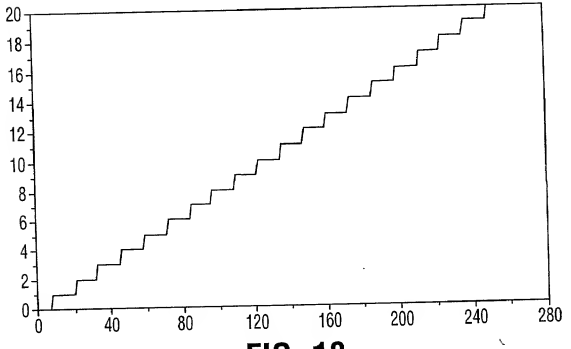

FIG. 18